What is claimed is:

1. A level-shifting input receiver circuit, the circuit comprising:

a differential amplifier having first and second input terminals, first and second output terminals, and first and second power terminals, where the first input terminal is configured to receive a first input data signal, the second input terminal is configured to receive a second input data signal, and the first power terminal is configured to receive a first power supply voltage;

a first current source having a first power terminal coupled to the second power terminal of the differential amplifier, a second power terminal configured to receive a second power supply voltage, and a control terminal configured to receive a bias control signal;

a first load having a first terminal configured to receive a third power supply voltage and a second terminal coupled to the first output terminal of the differential amplifier;

a second current source having a first power terminal coupled to the first output terminal of the differential amplifier, a second power terminal configured to receive the second power supply voltage, and a control terminal configured to receive the bias control signal;

a second load having a first terminal configured to receive the third power supply voltage and a second terminal coupled to the second output terminal of the differential amplifier; and

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a third current source having a first power terminal coupled to the second output terminal of the differential amplifier, a second power terminal configured to receive the second power supply voltage, and a control terminal configured to receive the bias control signal.

2. The circuit of claim 1, the circuit further comprising:

a first clamp circuit configured to shunt current between the first output terminal of the differential amplifier and the second power supply voltage; and

a second clamp circuit configured to shunt current between the second output terminal of the differential amplifier and the second power supply voltage.

3. The circuit of claim 1, where the differential amplifier further includes:

a first pushing current source configured to direct current from the first power supply voltage to the first output terminal of the differential amplifier; and

a second pushing current source configured to direct current from the first power supply voltage to the second output terminal of the differential amplifier; and

where the first and second current sources and sized larger than the first and second pushing current sources.

4. The circuit of claim 1, where:

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the first load further comprises a first PMOS device having a first current terminal configured to receive the third power supply voltage, a second current terminal coupled to the first output terminal of the differential amplifier, and a control terminal configured to receive the second power supply voltage; and

the second load further comprises a second PMOS device having a first current terminal configured to receive the third power supply voltage, a second current terminal coupled to the second output terminal of the differential amplifier, and a control terminal configured to receive the second power supply voltage.

5. The circuit of claim 1, where the differential amplifier further comprises:

a first NMOS transistor having a control terminal coupled to the first input terminal of the differential amplifier, a first current terminal, and a second current terminal coupled to the second power terminal of the differential amplifier;

a second NMOS transistor having a control terminal coupled to the second input terminal of the differential amplifier, a first current terminal, and a second current terminal coupled to the second power terminal of the differential amplifier;

a first PMOS transistor having a first current terminal coupled to the first power terminal of the differential amplifier, a control terminal coupled to a second current terminal, and where the second current terminal is coupled to the first current terminal of the first NMOS transistor;

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a second PMOS transistor having a first current terminal coupled to the first power terminal of the differential amplifier, a control terminal coupled to the control terminal of the first PMOS transistor, and a second current terminal coupled to the second output terminal of the differential amplifier;

a third PMOS transistor having a first current terminal coupled to the first power terminal of the differential amplifier, a control terminal coupled to the control terminal of the first PMOS transistor, and a second current terminal coupled to the first current terminal of the second NMOS transistor;

a fourth PMOS transistor having a first current terminal coupled to the first power terminal of the differential amplifier, a control terminal coupled to a second current terminal, where the second current terminal of the fourth PMOS transistor is coupled to the first current terminal of the first NMOS transistor;

a fifth PMOS transistor having a first current terminal coupled to the first power terminal of the differential amplifier, a control terminal coupled to the control terminal of the fourth PMOS transistor, and a second current terminal coupled to the first output terminal of the differential amplifier; and

a sixth PMOS transistor having a first current terminal coupled to the first power terminal of the differential amplifier, a control terminal coupled to the control terminal of the fourth PMOS transistor, and a second current terminal coupled to the first current terminal of the first NMOS transistor.

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6. The circuit of claim 1, where the second power supply voltage is greater in magnitude than the third power supply voltage.

7. The circuit of claim 1, where the third power supply voltage is less than twice a transistor threshold voltage.

8. The circuit of claim 1, where the second input data signal is complementary to the first input data signal.

9. The circuit of claim 1, where the second input data signal is a reference signal.

10. A method for level-shifting a received signal, the method comprising the steps of:

receiving first and second input signals having voltage levels related to an external power supply voltage;

differentially comparing the first and second input signals to generate a differential current signal, where the differential current signal is sourced from the external power supply voltage;

coupling a resistive load in series with a pulling current source between an internal power supply voltage and a ground supply voltage; and

driving the resistive load with the differential current signal.

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11. The method of claim 10, the method further including the step of clamping the differential current signal to the ground supply voltage.

12. The method of claim 10, where the step of differentially comparing the first and second input signals further comprises:

driving an NMOS differential pair with the first and second input signals to obtain an intermediate differential current signal; and

reflecting the intermediate differential current signal through a PMOS current mirror pair configured to draw current from the external power supply voltage in order to generate the differential current signal.

13. The method of claim 10, the method further including the step of sizing the pulling current source larger than the PMOS current mirror pair.

14. The method of claim 10, where the step of coupling a resistive load in series with a pulling current source further comprises:

coupling a first PMOS transistor in series with a first pulling current source between the internal power supply voltage and the ground supply voltage;

coupling a second PMOS transistor in series with a second pulling current source between the internal power supply voltage and the ground supply voltage;

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configuring the first and second PMOS transistors to operate in a linear range;

driving the first PMOS transistor with a non-inverted portion of the differential current signal; and

driving the second PMOS transistor with an inverted portion of the differential current signal.

15. The method of claim 10, the method including the step of configuring the external power supply voltage to be greater than the internal power supply voltage.

16. The method of claim 10, the method including the step of configuring the internal power supply voltage to be less than twice a transistor threshold voltage.

17. The method of claim 10, where the first and second input signals further comprise complementary data signals.

18. The method of claim 10, where the second input signal further comprises a reference voltage configured to differentiate between logic levels of the first input signal.

19. An apparatus for level-shifting a signal, the apparatus comprising:

an external power supply terminal, an internal power supply terminal, a ground supply terminal, first and second input terminals, and a bias input terminal;

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first, second and third current sources, each of the first, second and third current sources having first and second current terminals and a control terminal, where each of the first, second and third current sources is configured to conduct current between the first to the second current terminals under control of a signal received at the control terminal, and where the second current terminal of each of the first, second and third current sources is coupled to the ground supply terminal, and further wherein the control terminal of each of the first, second and third current sources is coupled to the bias input terminal;

a differential input buffer having a first input node coupled to the first input terminal, a second input node coupled to the second input terminal, a first power node coupled to the external power supply terminal, a second power node coupled to the first current terminal of the first current source, a first output terminal coupled to the first current terminal of the second current source, and a second output terminal coupled to the first current terminal of the third current source;

a first resistive load coupled between the internal power supply terminal and the first output terminal of the differential input buffer; and

a second resistive load coupled between the internal power supply terminal and the second output terminal of the differential input buffer.

20. The apparatus of claim 19, where the differential input buffer further comprises:

a first NMOS transistor having a gate coupled to the first input terminal, a source coupled to the first current terminal of the first current source, and a drain;

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a second NMOS transistor having a gate coupled to the second input terminal, a source coupled to the first current terminal of the first current source, and a drain;

a first PMOS transistor having a gate and a drain coupled to the drain of the first NMOS transistor, and a source coupled to the external power supply terminal;

a second PMOS transistor having a gate coupled to the gate of the first PMOS transistor, a source coupled to the external power supply terminal, and a drain coupled to the first output terminal of the differential input buffer;

a third PMOS transistor having a gate coupled to the gate of the first PMOS transistor, and a source coupled to the external power supply terminal, and a drain coupled to the drain of the second NMOS transistor;

a fourth PMOS transistor having a gate and a drain coupled to the drain of the second NMOS transistor, and a source coupled to the external power supply terminal;

a fifth PMOS transistor having a gate coupled to the gate of the fourth PMOS transistor, a source coupled to the external power supply terminal, and a drain coupled to the second output terminal of the differential input buffer; and

a sixth PMOS transistor having a gate coupled to the gate of the fourth PMOS transistor, and a source coupled to the external power supply terminal, and a drain coupled to the drain of the first NMOS transistor.

21. The apparatus of claim 19, where each of the first and second resistive loads further comprise a PMOS transistor configured to operate in its linear range.

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22. The apparatus of claim 19, the apparatus further including a clamp circuit having a first current terminal coupled to the first output terminal of the differential input buffer and a second current terminal coupled to the second output terminal of the differential input buffer, and a third current terminal coupled to the ground supply terminal, where the clamp circuit is configured to sink current from one of the first and second current terminals of the clamp circuit to the third current terminal of the clamp circuit responsive to the voltage at one of the first and second current terminals of the clamp circuit exceeding a predetermined voltage level.

23. The apparatus of claim 19, where the apparatus is configured to receive a greater voltage at the external power supply voltage terminal than a voltage received at the internal power supply voltage terminal.

24. The apparatus of claim 19, where the apparatus is configured to receive a voltage at the internal power supply voltage terminal that is less than twice a transistor threshold voltage.

25. The apparatus of claim 19, where the first and second input terminals are configured to receive first and second complementary data signals, respectively.

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26. The apparatus of claim 19, where the first input terminal is configured to receive a data signal and the second input terminal is configured to receive a reference voltage configured to differentiate between logic levels of the data signal.

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